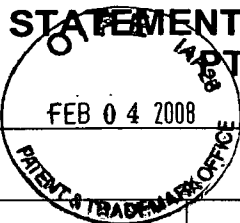


# INFORMATION DISCLOSURE STATEMENT BY APPLICANTS



Attorney Docket No.  
2885/56

Serial No.  
10/009,649

Applicant(s)  
Martin Vorbach et al.

Filing Date  
May 29, 2002

Group Art Unit  
2192

## U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
/TD/	RE34,444	November 1993	Kaplinsky			
	4,233,667	November 11, 1980	Devine et al.			
	4,414,547	November 1983	Knapp et al.			
	4,489,857	February 6, 1986	Agrawal et al.			
	4,590,583	May 20, 1986	Miller			
	4,882,687	November 1989	Gordon			
	4,918,440	April 17, 1990	Furtek et al.			
	5,072,178	December 10, 1991	Matsumoto			
	5,193,202	March 9, 1993	Jackson et al.			
	5,212,716	May 1993	Ferraiolo et al.			
	5,218,302	June 8, 1993	Loewe et al.			
	5,276,836	January 4, 1994	Fukumaru et al.			
	5,311,079	May 10, 1994	Ditlow et al.			
	5,392,437	February 21, 1995	Matter et al.			
	5,469,003	November 1995	Kean			
	5,581,731	December 3, 1996	King et al.			
	5,652,529	July 1997	Gould et al.			
	5,748,979	May 1998	Trimberger			
	5,752,035	May 1998	Trimberger			
	5,754,820	May 19, 1998	Yamagami			
	5,821,744	October 1998	Veytsman et al.			
	5,862,403	January 1999	Kanai et al.			
	5,892,962	April 6, 1999	Cloutier			
	5,960,193	September 28, 1999	Guttag et al.			
	5,978,583	November 1999	Ekanadham et al.			
	6,026,481	February 2000	New et al.			
	6,058,469	May 2, 2000	Baxter			
	6,077,315	June 2000	Greenbaum et a.			
	6,086,628	July 11, 2000	Dave et al.			
	6,105,106	August 2000	Manning			
	6,134,166	October 17, 2000	Lytle et al.			
	6,173,434	January 9, 2001	Wirthlin et al.			
	6,185,256	February 2001	Saito et al.			
	6,188,240	February 2001	Nakaya			
	6,198,304	March 2001	Sasaki			
	6,211,697	April 2001	Lien et al.			
	6,219,833	April 17, 2001	Solomon et al.			
	6,230,307	May 8, 2001	Davis et al.			

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

Attorney Docket No.  
2885/56

Serial No.  
10/009,649

Applicant(s)  
Martin Vorbach et al.

Filing Date  
May 29, 2002

Group Art Unit  
2192

/TD/	6,256,724	July 2001	Hocevar et al.			
	6,285,624	September 2001	Chen			
	6,321,373	November 20, 2001	Ekanadham et al.			
	6,400,601	June 2002	Sudo et al.			
	6,425,054	July 23, 2002	Nguyen			
	6,434,699	August 13, 2002	Jones et al.			
	6,435,054	October 10, 2000	Nguyen			
	6,437,441	August 2002	Yamamoto			
	6,476,634	November 2002	Bilski			
	6,504,398	April 2004	Vorbach			
	6,516,382	February 2003	Manning			
	6,518,787	February 2003	Allegrucci et al.			
	6,525,678	February 2003	Veenstra et al.			
	6,587,939	July 1, 2003	Takano			
	6,633,181	October 2003	Rupp			
	6,708,325	March 2004	Cooke et al.			
	6,721,830	April 2004	Vorbach et al.			
	6,728,871	April 27, 2004	Vorbach et al.			
	6,757,892	June 2004	Gokhale et al.			
	6,803,787	October 2004	Wicker, Jr.			
	6,871,341	March 2005	Shyr			
	6,886,092	April 2005	Douglass et al.			
	6,901,502	May 2005	Yano et al.			
	6,928,523	August 2005	Yamada, Akira			
	7,010,687	March 2006	Vorbach et al.			
	7,237,087	June 26, 2007	Vorbach et al.			
	7,254,649	August 2007	Subramanian et al.			
	2001/0010074	July 26, 2001	Nishihara et al.			
	2001/0032305	October 2001	Barry			
	2002/0103839	August 2002	Ozawa			
	2002/083308	June 27, 2002	Pereira et al.			
	2002/0045952	April 18, 2002	Blemel			
	2002/0138716	September 26, 2002	Paul et al.			
	2003/0001615	January 2003	Sueyoshi et al.			
	2003/0014743	January 16, 2003	Cooke et al.			
	2003/0086300	May 2003	Noyes et al.			
	2004/0168099	August 26, 2004	Vorbach et al.			
	2004/0199688	October 2004	Vorbach et al.			

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. 2885/56	Serial No. 10/009,649
	Applicant(s) Martin Vorbach et al.	
	Filing Date May 29, 2002	Group Art Unit 2192

**FOREIGN PATENT DOCUMENTS**

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
/TD/	0 208 457	January 14, 1987	EPO				
	0 398 552	November 22, 1009	EPO				
	0 696 001	December 5, 2001	EPO				
	0 735 685	October 2, 1996	EPO				
	0 746 106	December 4, 1996	EPO				
	2 752 466	February 20, 1998	France			English equivalent: USP 6,425,054 cited above	
	38 55 673	November 20, 1996	Germany			Abstract Only	
	WO92/01987	February 6, 1992	PCT				
	WO94/06077	March 17, 1994	PCT				
	WO99/00731	January 7, 1999	PCT				
	WO99/00739	January 7, 1999	PCT				
	WO99/12111	March 11, 1999	PCT				
	WO00/38087	June 29, 2000	PCT				
	WO01/55917	August 2, 2001	PCT				
	WO02/21010	March 14, 2002	PCT				
	WO02/071196	September 26, 2002	PCT				
	WO04/114128	December 29, 2004	PCT				
	8-44581	February 16, 1996	Japan			Abstract	
	7-154242	June 16, 1995	Japan			Abstract	
	58-58672	April 7, 1983	Japan			Abstract	
	2-226423	September 10, 1990	Japan			Abstract	
	5-276007	October 22, 1993	Japan			Abstract	
	8-250685	September 27, 1996	Japan			Abstract	
	2-130023	May 18, 1990	Japan			Abstract	
	11-307725	November 5, 1999	Japan			Abstract & Partial Translation	
	2000-181566	June 30, 2000	Japan			Computer Translation	
	9-27745	January 28, 1997	Japan			Abstract	
↓	05-509184		Japan			English Equivalent = USP 5,193,202 cited above	

**OTHER DOCUMENTS**

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. 2885/56	Serial No. 10/009,649
	Applicant(s) Martin Vorbach et al.	
	Filing Date May 29, 2002	Group Art Unit 2192

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
/TD/	Abnous, A., et al., "The Pleiades Architecture," Chapter I of <i>The Application of Programmable DSPs in Mobile Communications</i> , A. Gatherer and A. Auslander, Ed., Wiley, 2002, pp. 1-33.
	Alippi, et al., "Determining the Optimum Extended Instruction Set Architecture for Application Specific Reconfigurable VLIW CPUs," IEEE, 2001, pp. 50-56.
	Athanas, "A Functional Reconfigurable Architecture and Compiler for Adoptive Computing," IEEE 1993, pages 49-55.
	Athanas et al., "Processor Reconfiguration Through Instruction-Set Metamorphosis," 1993, IEEE Computers, pp. 11-18.
	Beck et al., "From control flow to data flow," TR 89-1050, October 1989, Dept. of Computer Science, Cornell University, Ithaca, NY, pp. 1-25.
	Callahan, et al., "The Garp Architecture and C Compiler," Computer, April 2000, pages 62-69.
	Cardoso, Joao M.P. and Markus Weinhardt, "XPP-VC: A C Compiler with Temporal Partitioning for the PACT-XPP Architecture," Field-Programmable Logic and Applications. Reconfigurable Computing is Going Mainstream, 12 <sup>th</sup> International Conference FPL 2002, Proceedings (Lecture Notes in Computer Science, Vol. 2438) Springer-Verlag Berlin, Germany, 2002, pp. 864-874.
	Chen et al., "A reconfigurable multiprocessor IC for rapid prototyping of algorithmic-specific high-speed DSP data paths," IEEE Journal of Solid-State Circuits, Vol. 27, No. 12, December 1992, pp.1895-1904.
	DeHon, A., "DPGA Utilization and Application," MIT Artificial Intelligence Laboratory, Proceedings of the Fourth International ACM Symposium on Field-Programmable Gate Arrays (FPGA '96), IEEE Computer Society, pp. 1-7.
	Dutt, et al., "If Software is King for Systems-in-Silicon, What's New in Compiler?," IEEE, 1997, pp. 322-325.
	Fornaciari, et al., System-level power evaluation metrics, 1997 Proceedings of the 2 <sup>nd</sup> Annual IEEE International Conference on Innovative Systems in Silicon, New York, NY, October 1997, pp. 323-330.
	Franklin, Manoj et al., "A Fill-Unit Approach to Multiple Instruction Issue," Proceedings of the Annual International Symposium on Microarchitecture, November 1994, pp. 162-171.
	Hartenstein, R., "Coarse grain reconfigurable architectures," Design Automation Conference, 2001, Proceedings of the ASP-DAC 2001 Asia and South Pacific, January 30- February 2, 2001, IEEE 30 January 2001, pp. 564-569.
	Hastie et al., "The implementation of hardware subroutines on field programmable gate arrays," Custom Integrated Circuits Conference, 1990, Proceedings of the IEEE 1990, May 16, 1990, pp. 31.3.1 – 31.4.3 (3 pages).
	Hedge, S.J., "3D WASP Devices for On-line Signal and Data Processing," 1994, International Conference on Wafer Scale Integration, pages 11-21.
	Hwang, K., "Advanced Computer Architecture – Parallelism, Scalability, Programmability," 1993, McGraw-Hill, Inc., pp. 348-355.
	IBM Technical Disclosure Bulletin, IBM Corp., New York, XP000424878, Bd. 36, Nr. 11, 1 November 1993, pp. 335-336.
	Iseli, C., et al. "A C++ Compiler for FPGA Custom Execution Units Synthesis," IEEE, 1995, pp. 173-179.
	Kastrup, B., "Automatic Hardware Synthesis for a Hybrid Reconfigurable CPU Featuring Philips CPLDs," Proceedings of the PACT Workshop on Reconfigurable Computing, 1998, pp. 5-10.
	Koren et al., "A data-driven VLSI array for arbitrary algorithms," IEEE Computer Society, Long Beach, CA Vol. 21, No. 10, 1 October 1988, pp. 30-34.
	Lee et al., "A new distribution network based on controlled switching elements and its applications," IEEE/ACT Trans. of Networking, Vol. 3, No. 1, pp. 70-81, February 1995.
	Lee, Jong-cun et al., "Reconfigurable ALU Array Architecture with Conditional Execution," International Soc. Design Conference (ISOOC) [online] October 25, 2004, Seoul, Korea, 5 pages.
	Ling, X., "WASMII: An MPLD with Data-Driven Control on a Virtual Hardware," Journal of Supercomputing, Kluwer Academic Publishers, Dordrecht, Netherlands, 1995, pp. 253-276.
	Ling et al., "WASMII: A Multifunction Programmable Logic Device (MPLD) with Data Driven Control," The Transactions of the Institute of Electronics, Information and Communication Engineers, 25 April 1994, Vol. J77-D-1, Nr. 4, pp. 309-317. [This references is in Chinese, but should be comparable in content to the Ling et al. reference above]
	Ozawa, Motokazu et al., "A Cascade ALU Architecture for Asynchronous Super-Scalar Processors," IEICE Transactions on Electronics, Electronics Society, Tokyo, Japan, Vol. E84-C, No. 2, February 2001, pp. 229-237.
V	Piotrowski, A., "IEC-BUS, Die Funktionsweise des IEC-Bus unde seine Anwendung in Geräten und Systemen," 1987, Franzis-Verlag GmbH, München, pp. 20-25.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. 2885/56	Serial No. 10/009,649
	Applicant(s) Martin Vorbach et al.	
	Filing Date May 29, 2002	Group Art Unit 2192

/TD/	Razdan et al., "A High-Performance Microarchitecture with Hardware-Programmable Functional Units, Micro-27, Proceedings of the 27 <sup>th</sup> Annual International Symposium on Microarchitecture, IEEE Computer Society and Association for Computing Machinery, November 30-December 2, 1994, pp. 172-180.
	Schmit, et al., Hidden Markov Modeling and Fuzzy Controllers in FPGAs, FPGAs for Custom Computing machines, 1995; Proceedings, IEEE Symposium in Napa Valley, CA, April 1995, pp. 214-221.
	Shirazi, et al., "Quantitative analysis of floating point arithmetic on FPGA based custom computing machines," IEEE Symposium on FPGAs for Custom Computing Machines, IEEE Computer Society Press, April 19-21, 1995, pp. 155-162.
	Siemers et al., "The >S<puter: A Novel Micoarchitecture Mode for Execution inside Superscalar and VLIW Processors Using Reconfigurable Hardware," Australian Computer Science Communications, Volume 20, No. 4, Computer Architecture, Proceedings of the 3 <sup>rd</sup> Australian Computer Architecture Conference, Perth, John Morris, Ed., February 2-3, 1998, pp. 169-178.
	Simunic, et al., Source Code Optimization and Profiling of Energy Consumption in Embedded Systems, Proceedings of the 13 <sup>th</sup> International Symposium on System Synthesis, September 2000, pp. 193-198.
	Skokan, Z.E., "Programmable logic machine (A programmable cell array)," IEEE Journal of Solid-State Circuits, Vol. 18, Issue 5, October 1983, pp. 572-578.
	Sueyoshi, T., "Present Status and Problems of the Reconfigurable Computing Systems Toward the Computer Evolution," Department of Artificial Intelligence, Kyushi Institute of Technology, Fukuoka, Japan; Institute of Electronics, Information and Communication Engineers, Vol. 96, No. 426, IEICE Technical Report (1996), pp. 111-119 [English Abstract Only]
	The XPP White Paper, Release 2.1, PACT - A Technical Perspective, March 27, 2002, pages 1-27.
	Villasenor, et al., "Express Letters Video Communications Using Rapidly Reconfigurable Hardware," IEEE Transactions on Circuits and Systems for Video Technology, IEEE, Inc., NY, December 1995, pp. 565-567.
	Weinhardt, M., "Compilation Methods for Structure-programmable Computers," dissertation, ISBN 3-89722-011-3, 1997. [TABLE OF CONTENTS AND ENGLISH ABSTRACT PROVIDED]
	Weinhardt, Markus et al., "Pipeline Vectorization," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 2, February 2001, pp. 234-248.
	XILINX, "Logic Cell Array Families: XC4000, XC4000A and XC4000H," product description, pp. 2-7, 2-9, 2-14, 2-15, 8-16, and 9-14.
	XILINX, "Spartan and SpartanXL Families Field Programmable Gate Arrays," January 1999, Xilinx, pp. 4-3 through 4-70.
	Ye, Z.A. et al., "A C-Compiler for a Processor With a Reconfigurable Functional Unit," FPGA 2000 ACM/SIGNA International Symposium on Field Programmable Gate Arrays, Monterey, CA Feb 9-11, 2000, pp. 95-100.
	Yeung, A. et al., "A data-driven architecture for rapid prototyping of high throughput DSP algorithms," Dept. of Electrical Engineering and Computer Sciences, Univ. of California, Berkeley, USA, <i>Proceedings VLSI Signal Processing Workshop, IEEE Press</i> , pp. 225-234, Napa, October 1992.
	Yeung, A. et al., "A reconfigurable data-driven multiprocessor architecture for rapid prototyping of high throughput DSP algorithms," Dept. of Electrical Engineering and Computer Sciences, Univ. of California, Berkeley, USA, pp. 169-178, <i>IEEE</i> 1993.
	Zhang, et al., Architectural Evaluation of Flexible Digital Signal Processing for Wireless Receivers, Signals, Systems and Computers, 2000; Conference Record of the Thirty-Fourth Asilomar Conference, Bd. 1, 29 October 2000, pp. 78-83.

EXAMINER	/Thuy Dao/	DATE CONSIDERED	04/20/2008
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			